

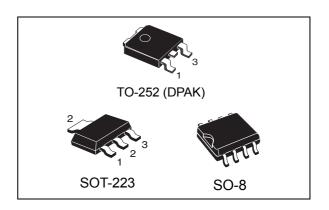
# VND1NV04 VNN1NV04 - VNS1NV04

OMNIFET II fully autoprotected Power MOSFET

#### **Features**

Parameter	Symbol	Value
Max on-state resistance (per ch.)	R <sub>ON</sub>	250 mΩ
Current limitation (typ)	I <sub>LIMH</sub>	1.7 A
Drain-source clamp voltage	$V_{CLAMP}$	40 V

- Linear current limitation
- Thermal shutdown
- Short circuit protection
- Integrated clamp
- Low current drawn from input pin
- Diagnostic feedback through input pin
- ESD protection
- Direct access to the gate of the Power MOSFET (analog driving)
- Compatible with standard Power MOSFET



#### **Description**

The VND1NV04, VNN1NV04, VNS1NV04 are monolithic devices designed in STMicroelectronics® VIPower® M0-3 Technology, intended for replacement of standard Power MOSFETs from DC up to 50 KHz applications. Built in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments.

Fault feedback can be detected by monitoring the voltage at the input pin.

Table 1. Device summary

Packago		O	rder codes	
Package Tube		Tube (lead free)	Tape and reel	Tape and reel (lead free)
TO-252 (DPAK)	VND1NV04	VND1NV04-E	VND1NV0413TR	VND1NV04TR-E
SOT-223	VNN1NV04	-	VNN1NV0413TR	-
SO-8	VNS1NV04	-	VNS1NV0413TR	-

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## 1 Block diagram and pin description

Figure 1. Block diagram

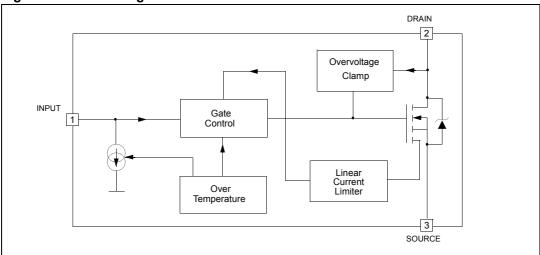
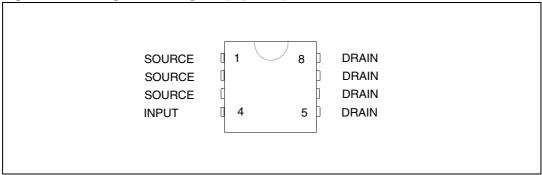


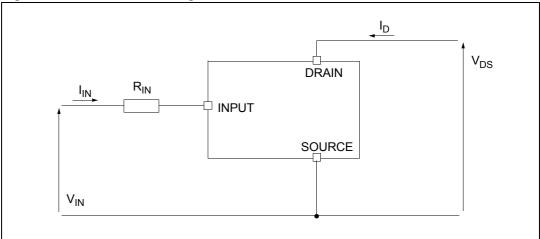
Figure 2. Configuration diagram (top view)



1. For the pins configuration related to SOT-223 and DPAK see outline at page 1.

### 2 Electrical specifications

Figure 3. Current and voltage conventions



### 2.1 Absolute maximum ratings

The rating listed in *Table 2: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to Absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value			Unit
Symbol	Farameter	SOT-223	SO-8	DPAK	Unit
$V_{DSn}$	Drain-source voltage (V <sub>INn</sub> =0 V) Internally clamped		ped	V	
V <sub>INn</sub>	Input voltage	Inte	rnally clam	ped	V
I <sub>INn</sub>	Input current		+/-20		mA
R <sub>IN MINn</sub>	Minimum input series impedance	330		Ω	
I <sub>Dn</sub>	Drain current	Internally limited		Α	
I <sub>Rn</sub>	Reverse DC output current	-3		Α	
V <sub>ESD1</sub>	Electrostatic discharge (R=1.5 KΩ, C=100 pF)	4000		V	
V <sub>ESD2</sub>	Electrostatic discharge on output pins only (R=330 $\Omega$ , C=150 pF)	16500		٧	
P <sub>tot</sub>	Total dissipation at T <sub>c</sub> =25 °C	7 8.3 35		35	W
Tj	Operating junction temperature Internally limited		°C		
T <sub>c</sub>	Case operating temperature	Internally limited		°C	
T <sub>stg</sub>	Storage temperature		-55 to 150		°C

### 2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Ma	Unit		
Symbol	raiametei	SOT-223	SO-8	DPAK	Oilit
R <sub>thj-case</sub>	Thermal resistance junction-case	18		3.5	°C/W
R <sub>thj-lead</sub>	Thermal resistance junction-lead		15		°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-ambient	70 <sup>(1)</sup>	65 <sup>(1)</sup>	54 <sup>(1)</sup>	°C/W

<sup>1.</sup> When mounted on a standard single-sided FR4 board with 50 mm $^2$  of Cu (at least 35  $\mu$ m thick) connected to all DRAIN pins

#### 2.3 Electrical characteristics

Table 4. Electrical characteristics

	Licotrical characteristics						
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit	
Off (-40 °C <tj<150 otherwise="" specified)<="" td="" unless="" °c,=""></tj<150>							
V <sub>CLAMP</sub>	Drain-source clamp voltage	V <sub>IN</sub> =0 V; I <sub>D</sub> =0.5 A	40	45	55	V	
V <sub>CLTH</sub>	Drain-source clamp threshold voltage	V <sub>IN</sub> =0 V; I <sub>D</sub> =2 mA	36			V	
$V_{INTH}$	Input threshold voltage	V <sub>DS</sub> =V <sub>IN</sub> ; I <sub>D</sub> =1 mA	0.5		2.5	٧	
I <sub>ISS</sub>	Supply current from input pin	V <sub>DS</sub> =0 V; V <sub>IN</sub> =5 V		100	150	μΑ	
V	Input-source clamp	I <sub>IN</sub> =1 mA	6	6.8	8	V	
V <sub>INCL</sub> voltage	voltage	I <sub>IN</sub> =-1 mA	-1.0		-0.3		
	Zero input voltage	V <sub>DS</sub> =13 V; V <sub>IN</sub> =0 V; T <sub>j</sub> =25 °C			30	μΑ	
I <sub>DSS</sub>	drain current (V <sub>IN</sub> =0 V)	V <sub>DS</sub> =25 V; V <sub>IN</sub> =0 V			75		
On (-40 °	C <tj<150 of<="" td="" unless="" °c,=""><td>herwise specified)</td><td></td><td></td><td></td><td></td></tj<150>	herwise specified)					
Б	Static drain-source on	V <sub>IN</sub> =5 V; I <sub>D</sub> =0.5 A; T <sub>j</sub> =25 °C			250	mΩ	
R <sub>DS(on)</sub> resistance		V <sub>IN</sub> =5 V; I <sub>D</sub> =0.5 A			500		
Dynamic (T <sub>j</sub> =25 °C, unless otherwise specified)							
g <sub>fs</sub> <sup>(1)</sup>	Forward transconductance	V <sub>DD</sub> =13 V; I <sub>D</sub> =0.5 A		2		S	
C <sub>OSS</sub>	Output capacitance	V <sub>DS</sub> =13 V; f=1 MHz; V <sub>IN</sub> =0 V		90		pF	
	•				•		

Table 4. Electrical characteristics (continued)

Table 4. Electrical characteristics (continued)						
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
Switching (T <sub>j</sub> =25 °C, unless otherwise specified)						
t <sub>d(on)</sub>	Turn-on delay time			70	200	ns
t <sub>r</sub>	Rise time	V <sub>DD</sub> =15 V; I <sub>D</sub> =0.5 A		170	500	ns
t <sub>d(off)</sub>	Turn-off delay time	$V_{gen}$ =5 V; $R_{gen}$ = $R_{IN MIN}$ =330 Ω (see <i>Figure 4</i> )		350	1000	ns
t <sub>f</sub>	Fall time	, (333 )		200	600	ns
t <sub>d(on)</sub>	Turn-on delay time			0.25	1.0	μs
t <sub>r</sub>	Rise time	V <sub>DD</sub> =15 V; I <sub>D</sub> =0.5 A		1.3	4.0	μs
t <sub>d(off)</sub>	Turn-off delay time	$V_{gen}$ =5 V; R <sub>gen</sub> =2.2 KΩ (see <i>Figure 4</i> )		1.8	5.5	μs
t <sub>f</sub>	Fall time	(coo i igano i)		1.2	4.0	μs
(dl/dt) <sub>on</sub>	Turn-on current slope	$V_{DD}$ =15 V; $I_{D}$ =1.5 A $V_{gen}$ =5 V; $R_{gen}$ = $R_{IN\ MIN}$ =330 Ω		5		A/μs
Q <sub>i</sub>	Total input charge	V <sub>DD</sub> =12 V; I <sub>D</sub> =0.5 A; V <sub>IN</sub> =5 V I <sub>gen</sub> =2.13 mA (see <i>Figure 7</i> )		5		nC
Source d	rain diode (T <sub>j</sub> =25 °C, u	nless otherwise specified)				
V <sub>SD</sub> <sup>(1)</sup>	Forward on voltage	I <sub>SD</sub> =0.5 A; V <sub>IN</sub> =0 V		0.8		V
t <sub>rr</sub>	Reverse recovery time			205		ns
Q <sub>rr</sub>	Reverse recovery charge	I <sub>SD</sub> =0.5 A; dl/dt=6 A/μs V <sub>DD</sub> =30 V; L=200 μH		100		nC
I <sub>RRM</sub>	Reverse recovery current	(see <i>Figure 5</i> )		0.7		Α
Protectio	ns (-40 °C <t<sub>j&lt;150 °C,</t<sub>	unless otherwise specified)				
I <sub>lim</sub>	Drain current limit	V <sub>IN</sub> =5 V; V <sub>DS</sub> =13 V	1.7		3.5	Α
t <sub>dlim</sub>	Step response current limit	V <sub>IN</sub> =5 V; V <sub>DS</sub> =13 V		2.0		μs
T <sub>jsh</sub>	Overtemperature shutdown		150	175	200	°C
T <sub>jrs</sub>	Overtemperature reset		135			°C
I <sub>gf</sub>	Fault sink current	V <sub>IN</sub> =5 V; V <sub>DS</sub> =13 V; T <sub>j</sub> =T <sub>jsh</sub>	10	15	20	mA
E <sub>as</sub>	Single pulse avalanche energy	Starting T <sub>j</sub> =25 °C; V <sub>DD</sub> =24 V $V_{IN}$ =5 V R <sub>gen</sub> =R <sub>IN MIN</sub> =330 $\Omega$ ; L=50 mH (see <i>Figure 6</i> and <i>Figure 8</i> )	55			mJ
	1	1	L	·	l	

<sup>1.</sup> Pulsed: pulse duration = 300  $\mu$ s, duty cycle 1.5 %

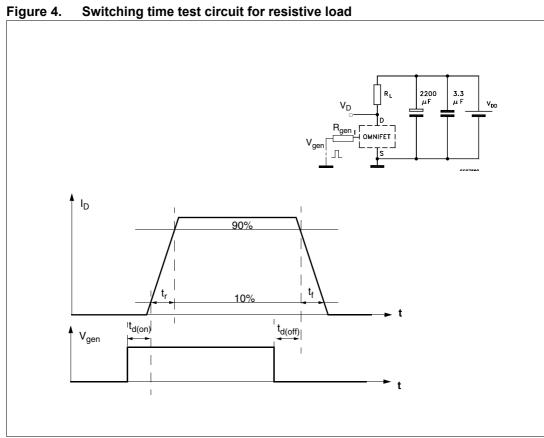
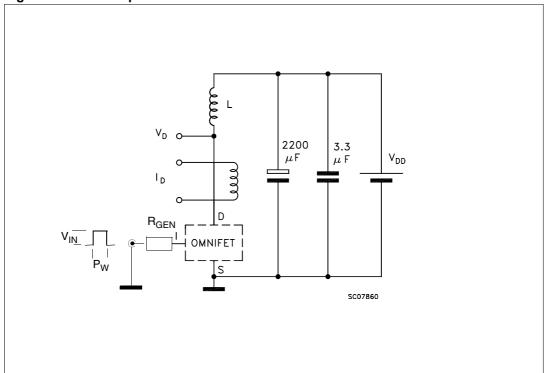


Figure 5. Test circuit for diode recovery times

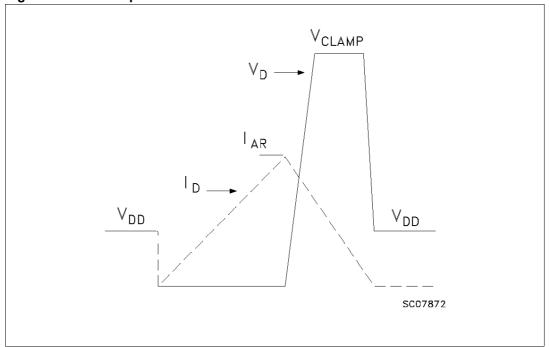




 $-^{\mathsf{V}_{\mathsf{DD}}}$ 47Κ Ω 100nF I = CONST 100Ω -I OMNIFET Ì D.U.T. 2200 ⊒ μF 2.7ΚΩ 

Figure 7. Input charge test circuit

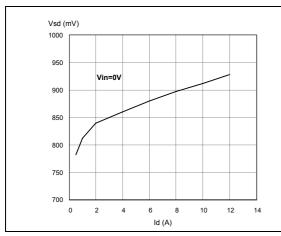




#### 2.4 Electrical characteristics curves

Figure 9. Source-drain diode forward characteristics

Figure 10. Static drain-source on resistance



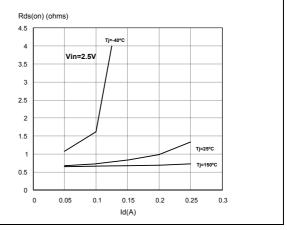
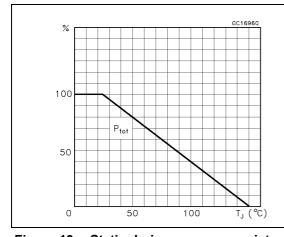


Figure 11. Derating curve

Figure 12. Static drain-source on resistance vs. input voltage (part 1/2)



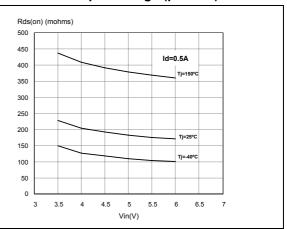
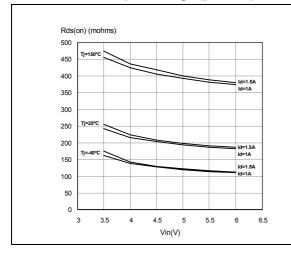
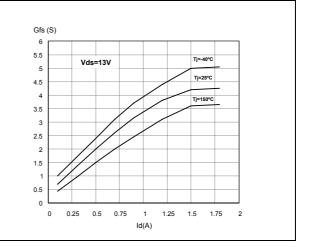


Figure 13. Static drain-source on resistance vs. input voltage (part 2/2)

Figure 14. Transconductance

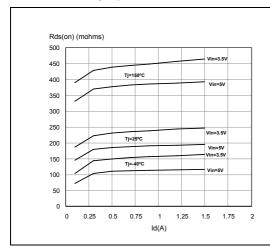




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Figure 15. Static drain-source on resistance Figure vs. Id

Figure 16. Transfer characteristics



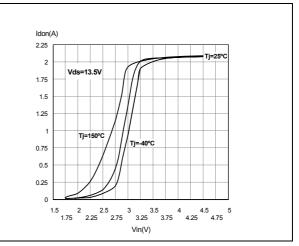
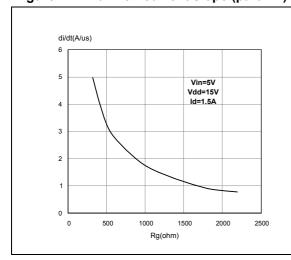


Figure 17. Turn-on current slope (part 1/2)

Figure 18. Turn-on current slope (part 2/2)



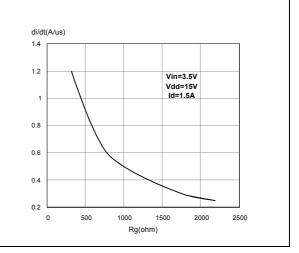
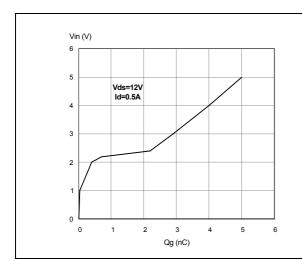
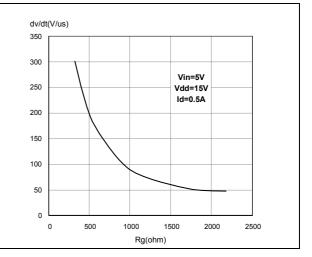


Figure 19. Input voltage vs. input charge

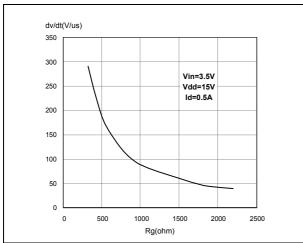
Figure 20. Turn-off drain source voltage slope (part 1/2)





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Figure 21. Turn-off drain-source voltage slope Figure 22. Capacitance variations (part 2/2)



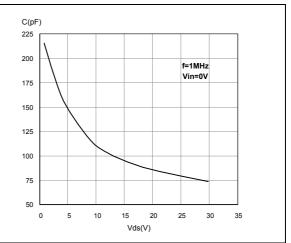
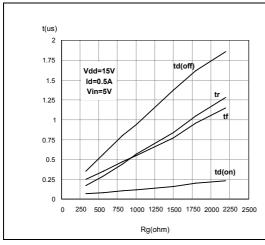


Figure 23. Switching time resistive load (part 1/2)

Figure 24. Switching time resistive load (part 2/2)



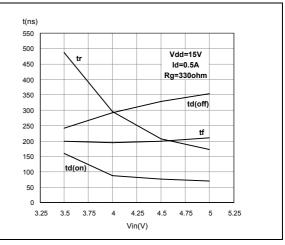
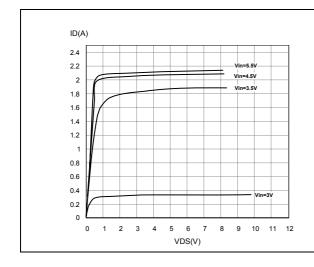
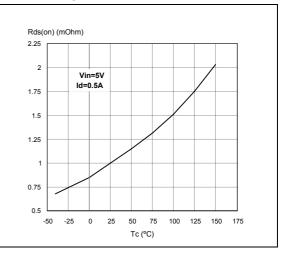


Figure 25. Output characteristics

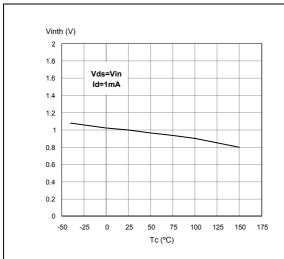
Figure 26. Normalized on resistance vs. temperature





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Figure 27. Normalized input threshold voltage Figure 28. Normalized current limit vs. vs. temperature junction temperature



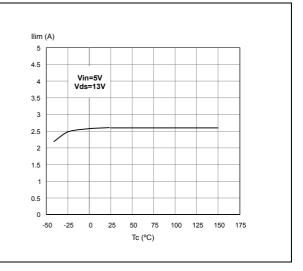
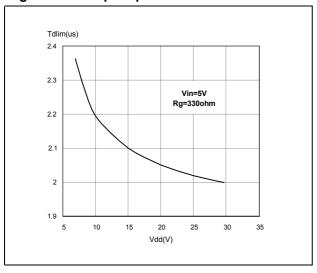


Figure 29. Step response current limit



#### 3 Protection features

During normal operation, the input pin is electrically connected to the gate of the internal Power MOSFET through a low impedance path.

The device behaves like a standard Power MOSFET and it can be used as a switch from DC up to 50 KHz. The only difference from the user's point of view is that a small DC current  $I_{ISS}$  (typ. 100  $\mu$ A) flows into the input pin in order to supply the internal circuitry.

The device integrates:

- Overvoltage clamp protection gives
  - Internally set at 45 V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.
- Linear current limiter circuit
  - Limits the drain current I<sub>D</sub> to I<sub>lim</sub> whatever the input pin voltages. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the overtemperature threshold T<sub>ish</sub>.
- Overtemperature and short circuit protection
  - These are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Overtemperature cutout ranges is from 150 to 190 °C, a typical value is 170 °C. The device is automatically restarted when the chip temperature falls of about 15 °C below shutdown temperature.

#### Status feedback

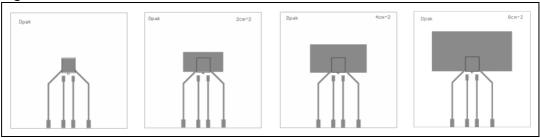
In the case of an overtemperature fault condition (T<sub>j</sub> > T<sub>jsh</sub>), the device tries to sink a diagnostic current I<sub>gf</sub> through the input pin in order to indicate fault condition. If driven from a low impedance source, this current may be used in order to warn the control circuit of a device shutdown. If the drive impedance is high enough so that the input pin driver is not able to supply the current I<sub>gf</sub>, the input pin falls to 0 V. This does not however affect the device operation: no requirement is put on the current capability of the input pin driver except to be able to supply the normal operation drive current I<sub>ISS</sub>. Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL logic circuit.

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### 4 Package and PCB thermal data

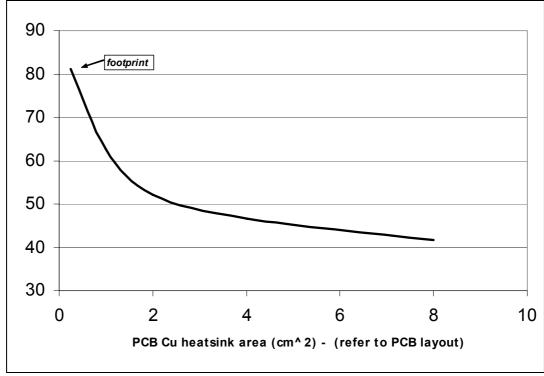
#### 4.1 DPAK thermal data

Figure 30. DPAK PC board



<sup>1.</sup> Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB FR4 area = 58 mm x 58 mm,PCB thickness = 2 mm, Cu thickness=35  $\mu$ m, Copper areas: from minimum pad layout to 16 cm<sup>2</sup>).

Figure 31. DPAK  $R_{thj-amb}$  vs. PCB copper area in open box free air condition



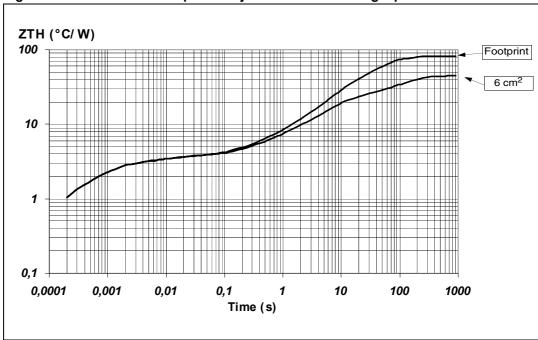


Figure 32. DPAK thermal impedance junction ambient single pulse

**Equation 1: Pulse calculation formula** 

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp} (1 - \delta)$$
  
where  $\delta = t_P/T$ 

Figure 33. DPAK thermal fitting model of a single channel

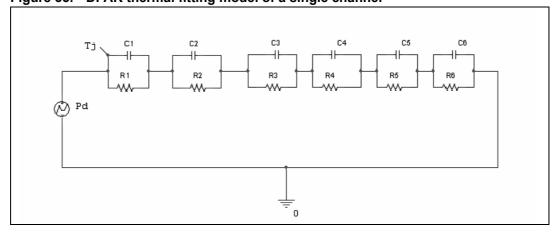
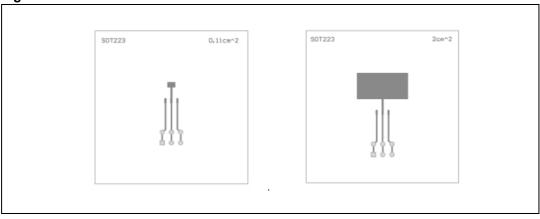


Table 5. DPAK thermal parameter

Area/island (cm <sup>2</sup> )	0.25	6
R1 (°C/W)	0.8	
R2 (°C/W)	1.6	
R3 (°C/W)	0.8	
R4 (°C/W)	2	
R5 (°C/W)	15	
R6 (°C/W)	61	24
C1 (W·s/°C)	0.00006	
C2 (W·s/°C)	0.0005	
C3 (W·s/°C)	0.01	
C4 (W·s/°C)	0.3	
C5 (W·s/°C)	0.45	
C6 (W·s/°C)	0.8	5

#### 4.2 SOT-223 thermal data

Figure 34. SOT-223 PC board



<sup>1.</sup> Layout condition of R $_{th}$  and Z $_{th}$  measurements (PCB FR4 area = 58 mm x 58 mm,PCB thickness = 2 mm, Cu thickness=35  $\mu$ m , Copper areas: from minimum pad layout to 0.8 cm<sup>2</sup>).

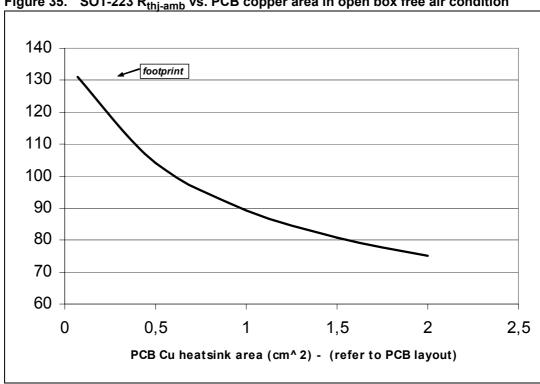
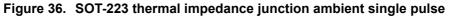
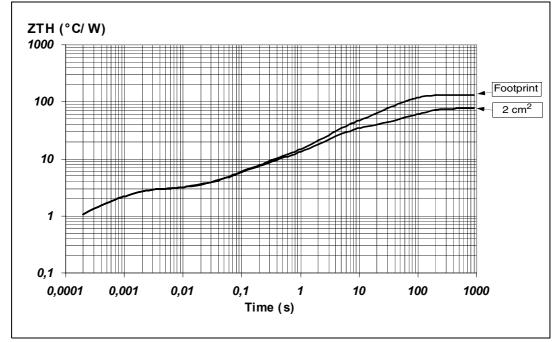


Figure 35. SOT-223 R<sub>thi-amb</sub> vs. PCB copper area in open box free air condition





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#### **Equation 2: Pulse calculation formula**

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp} (1 - \delta)$$
  
where  $\delta = t_P/T$ 

Figure 37. SOT-223 thermal fitting model of a single channel

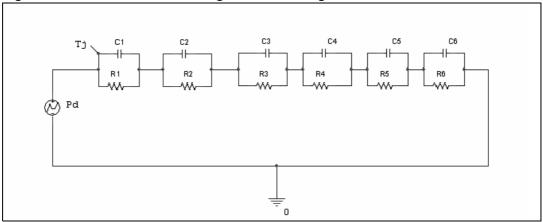
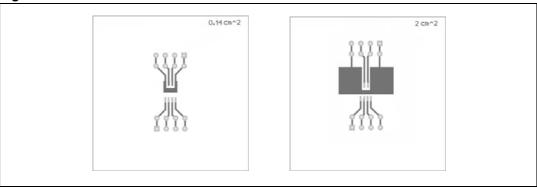


Table 6. SOT-223 thermal parameter

Area/island (cm <sup>2</sup> )	FP	2
R1 (°C/W)	0.8	
R2 (°C/W)	1.6	
R3 (°C/W)	4.5	
R4 (°C/W)	24	
R5 (°C/W)	0.1	
R6 (°C/W)	100	45
C1 (W·s/°C)	0.00006	
C2 (W·s/°C)	0.0005	
C3 (W·s/°C)	0.03	
C4 (W·s/°C)	0.16	
C5 (W·s/°C)	1000	
C6 (W·s/°C)	0.5	2

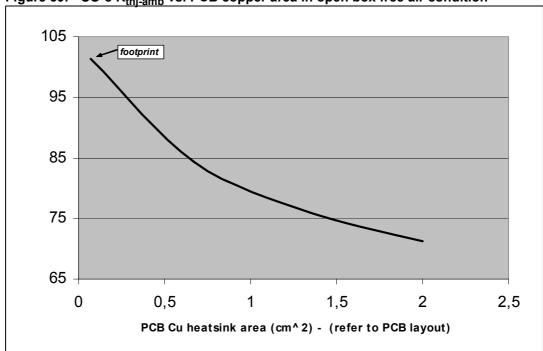
### 4.3 SO-8 thermal data

Figure 38. SO-8 PC board



1. Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB FR4 area = 58 mm x 58 mm,PCB thickness = 2 mm, Cu thickness=35  $\mu$ m, Copper areas: from minimum pad layout to 2 cm<sup>2</sup>).

Figure 39. SO-8  $R_{thi-amb}$  vs. PCB copper area in open box free air condition



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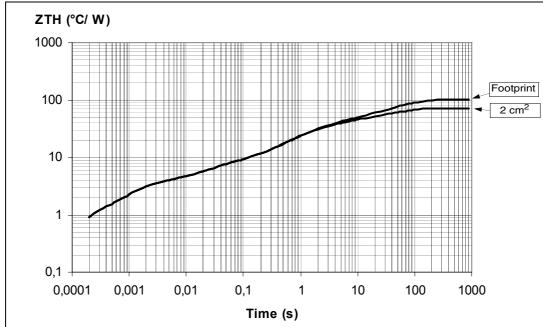


Figure 40. SO-8 thermal impedance junction ambient single pulse

**Equation 3: Pulse calculation formula** 

$$\begin{split} Z_{TH\delta} &= R_{TH} \cdot \delta + Z_{THtp} (1 - \delta) \\ \text{where } \delta &= t_P / T \end{split}$$

Figure 41. SO-8 thermal fitting model of a single channel

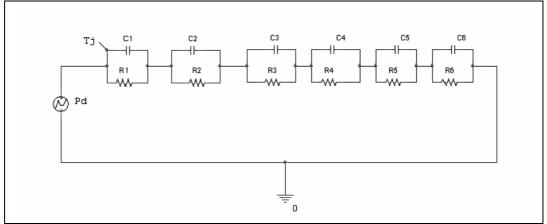


Table 7. SO-8 thermal parameter

Area/island (cm <sup>2</sup> )	FP	2
R1 (°C/W)	0.8	
R2 (°C/W)	2.6	
R3 (°C/W)	3.5	
R4 (°C/W)	21	
R5 (°C/W)	16	
R6 (°C/W)	58	28
C1 (W·s/°C)	0.00006	
C2 (W·s/°C)	0.0005	
C3 (W·s/°C)	0.0075	
C4 (W·s/°C)	0.045	
C5 (W·s/°C)	0.35	
C6 (W·s/°C)	1.05	2

### 5 Package and packing information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: <u>www.st.com</u>.

ECOPACK® is an ST trademark.

#### 5.1 DPAK mechanical data

Figure 42. DPAK package dimensions

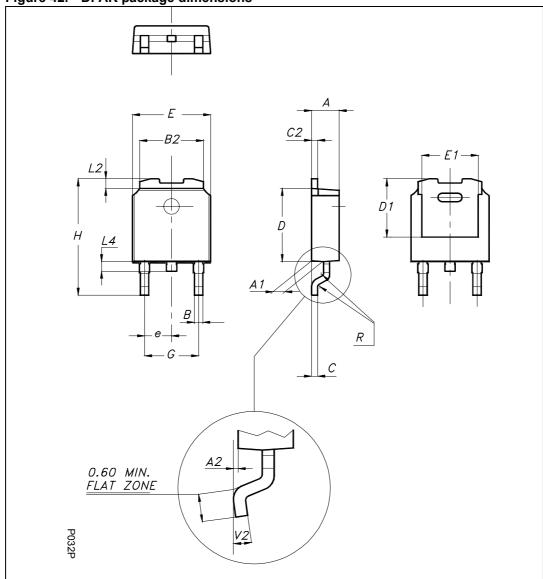
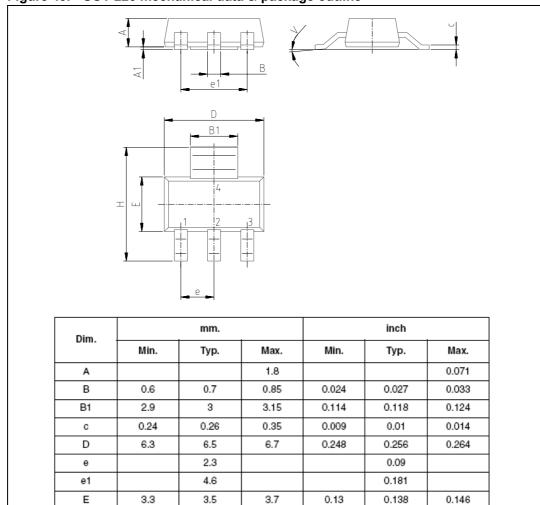


Table 8. DPAK mechanical data

Dim.	mm.		
	Min.	Тур.	Max.
Α	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
В	0.64		0.90
B2	5.20		5.40
С	0.45		0.60
C2	0.48		0.60
D	6.00		6.20
D1		5.1	
E	6.40		6.60
E1		4.7	
е		2.28	
G	4.40		4.60
Н	9.35		10.10
L2		0.8	
L4	0.60		1.00
R		0.2	
V2	0°	8°	
Package weight		Gr. 0.29	

#### 5.2 SOT-223 mechanical data

Figure 43. SOT-223 mechanical data & package outline



#### 5.3 SO8 mechanical data

H V

Α1

Table 9. SO-8 mechanical data

6.7

0.02

7

Dim.	mm		
	Min.	Тур.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		

7.3

0.1

10° (max)

0.264

0.0008

0.276

0.287

0.004

Table 9. SO-8 mechanical data (continued)

Dim.	mm			
	Min.	Тур.	Max.	
b	0.28		0.48	
С	0.17		0.23	
D <sup>(1)</sup>	4.80	4.90	5.00	
E	5.80	6.00	6.20	
E1 <sup>(2)</sup>	3.80	3.90	4.00	
е		1.27		
h	0.25		0.50	
L	0.40		1.27	
L1		1.04		
k	0°		8°	
ccc			0.10	

Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm in total (both side).

Figure 44. SO-8 package dimension

D

hx45

C

SEATING
PLANE
C

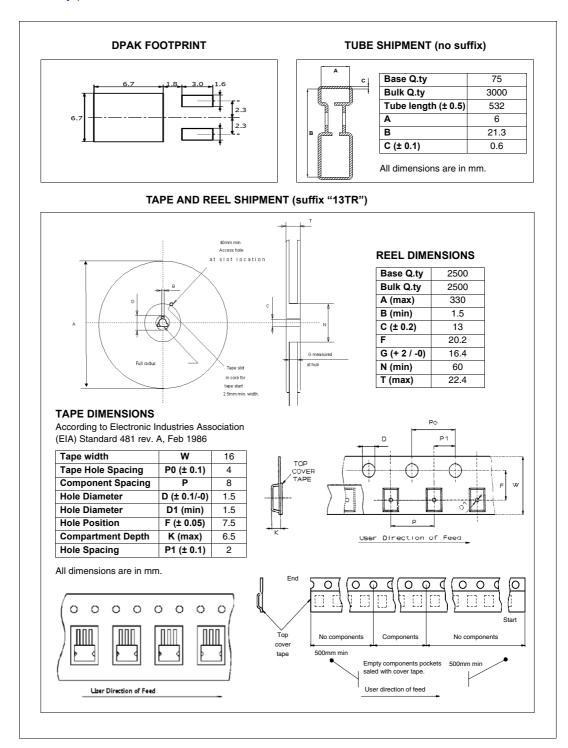
GAGE PLANE

0016023 D

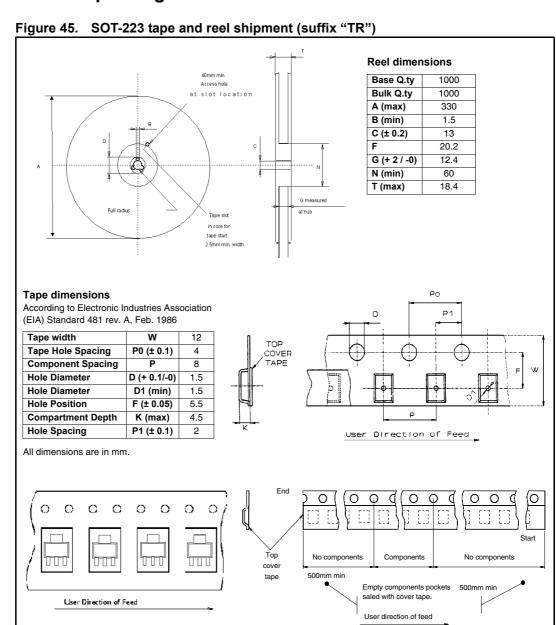
<sup>2.</sup> Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.

#### 5.4 DPAK packing information

The devices can be packed in tube or tape and reel shipments (see the *Table 1: Device summary* ).



### 5.5 SOT-223 packing information



### 5.6 SO8 packing information

Figure 46. SO-8 tube shipment (no suffix)

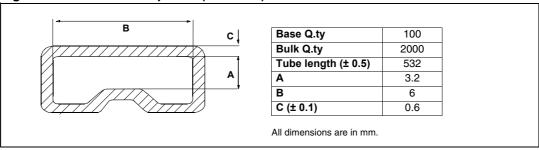
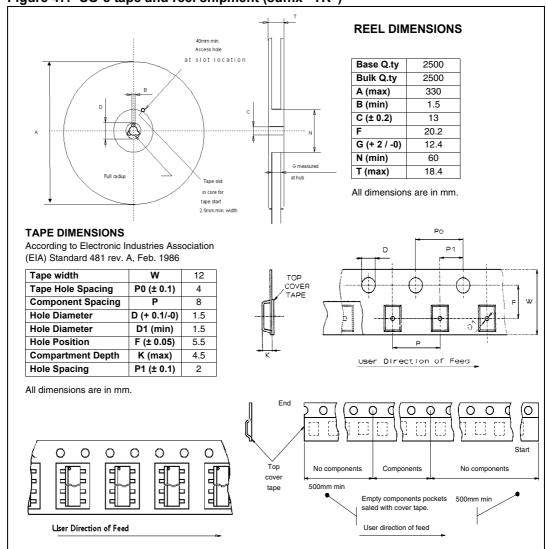


Figure 47. SO-8 tape and reel shipment (suffix "TR")



# 6 Revision history

Table 10. Document revision history

Date	Revision	Changes
Feb-2003	1	Initial release.
16-Apr-2009	2	Added Table 1: Device summary and Section 4: Package and PCB thermal data Updated Section 5: Package and packing information on page 25
01-Dic-2011	3	Upadate <i>Table 1: Device summary</i> . Update the entire document using the new coorporate template.

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